REMARKS

After entry of the present amendments, Claims 1-26 are pending in the present application and remain in this application for prosecution. Claims 1, 7, 14-16, 19-20, and 22-24 have been amended. Claims 25 and 26 have been added.

Introduction

Applicants' invention is generally directed to a low-power, low-voltage system bus that carries a number of signals over a fewer number of wires than the number of signals. Thus, for example, four signals are carried on a three-wire bus. Several examples include a composite line 32 (shown in FIG. 2a) that carries both CLOCK and VDD signals on a single wire. (See FIG. 2a; ¶¶ 43-44.) Another example is the composite line 34 that carries both DATA and SYNC signals on a single wire. (FIG. 2a; ¶ 45.) Other examples include combining CLOCK and SYNC signals on a single wire, ¶ 93, combining POWER and SYNC signals on a single wire, ¶ 95, combining POWER and DATA signals on a single wire, ¶ 96. Still other examples combine three or more signals on a single wire, such as combining the POWER, CLOCK, and SYNC signals on a single wire or the CLOCK, DATA, and SYNC signals on a single wire (¶ 97).

The term "composite line" as used in connection with embodiments of Applicants' specification is intended to convey that more than one signal is carried on a single line—not that the line itself is composed of more than one line. Such an interpretation would be self-contradictory. Rather, the "composite" nature of the line stems from the fact that on a single line more than one signal is carried.

Applicants have amended independent claim 1 to call for a system bus coupled to said at least one peripheral device, said system bus including at least two signal-carrying lines, one of

said lines carrying a digital signal and at least one other electrical signal ~~being a composite line adapted to carry more than one digital signal~~ between said master component and said at least one peripheral device, said one of said lines being termed a composite line.

Applicants now turn to the claim rejections.

Section 102 Rejections

Claims 1-4, 6-9, 13-16, 20, and 22-24 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,144,748 (Kerns). Applicants respectfully traverse these rejections.

The Office Action identifies the claimed system bus as corresponding to the common bus 217 and the audio bus 223, and identifies the composite line as "(elements 214, "CLOCK", "DATA")". Office Action at 3. As FIG. 3 (reproduced below for the Examiner's convenience) clearly shows, the input to the interface 219 is comprised of **four-wires** 214, one of which carries a CLOCK signal and another of which carries a DATA signal. Nothing in Kerns teaches that a single wire can carry both a CLOCK and a DATA signal as the Office Action seems to suggest by the cryptic quotation set forth above.

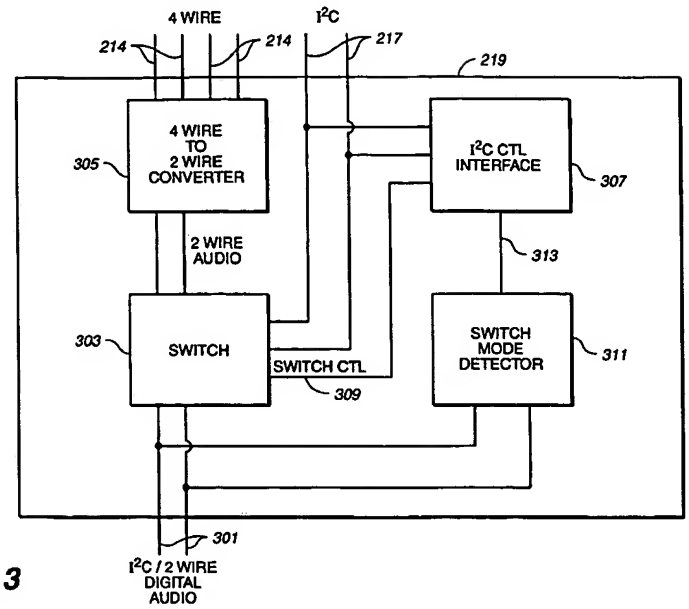

FIG._3

The identification of the elements 214 as corresponding to the claimed composite line is problematic for a couple of reasons. First, the Examiner is combining multiple, disparate, busses as comprising the claimed "system" bus. The alleged "system" bus includes the **common bus 217** connected between the DSP 213, the analog chip 211, the interface 219, and the EEPROM 215, **the audio bus 223** connected between the DSP 213 and the analog chip 211, and the **four-wire digital audio bus 214** connected between the DSP 213 and the interface 219. These three busses do not constitute a system bus as claimed.

Second, elements 214 cited by the Office Action is actually a "four-wire digital audio bus 214" as stated in column 3, line 28 of Kerns. One of the wires carries a CLOCK signal (see FIG. 2a) and another of the wires carries separately a DATA signal. There is no disclosure in Kerns that a single wire can carry both the CLOCK and DATA signals. The CLOCK wire of the four-wire audio bus 214 within the hearing device 210 always carries a CLOCK signal only, and the DATA wire of the four-wire audio bus 214 always carries a DATA signal only. In short, the elements 214 ("CLOCK", "DATA") do not constitute the claimed system bus including at least

two signal-carrying lines, one of said lines carrying a digital signal and at least one other electrical signal between said master component and said at least one peripheral device. If the rejection in view of Kerns is maintained, the Examiner is kindly requested in the next Office Action to identify where Kerns discloses any wire that carries a digital signal and at least one other electrical signal.

Turning now to the rejections of the dependent claims, Applicants traverse them a follows. Regarding claim 4, wherein said system bus is coupled to one of a resistor and a current source, the Office Action referred to Table 1. However, Table 1, which provides that the CLOCK line and DATA line are each connected via a pullup to a battery voltage V+, however the description at column 4, lines 53-54 makes it clear that Table 1 is directed to the functions of the pins of the **external** connector 221 (see FIG. 1d). For example, pin V+ is connected to a battery, which is also external to the hearing device 210. By contrast, claim 4 calls for a "portable communication device" in which the system bus is coupled to a resistor or a current source. In other words, the portable communication device includes a resistor or current source coupled to an internal system bus. In Kerns, the pullup connections to V+ are made external to the hearing device 210.

Regarding claim 7, which recites wherein said digital signal is a data signal that is time multiplexed into blocks having a number of frames, each frame having at least one data slot, Kerns does not disclose any such data signal. The two-wire protocol referred to in FIG. 4 is a "simple and involves little overhead"—in other words, it is a simple two-wire point-to-point protocol. Moreover, the two-wire protocol referred to in FIG. 4 (constituting the two-wire connection between the external connector 221 and the external digital interface chip 242 shown in FIG. 2), does not constitute the claimed system bus as one wire is used for the CLOCK signal

only and the other wire is used for the DATA signal only. A simple two-wire point-to-point protocol does not constitute the claimed time-multiplexed multiple-signal-carrying composite wire protocol called for by claim 4.

Regarding claim 8, Applicants traverse this rejection for at least the same reasons provided above in connection with claim 7. The two-wire I^2C bus described in Table 2 does not correspond to the claimed system bus. The I^2C bus is well known and contains a CLOCK line (SCL) and a serial DATA line (SDL). If rejection of claims 7-8 is maintained, the Examiner is invited to point out where in the I^2C bus specification there is provisioning for time-multiplexing of data into multi-frame blocks. Kerns does not disclose a system bus in which one of the lines carries a data signal that is time multiplexed into multi-frame blocks, each frame including a control slot carrying control data between the master component and a peripheral device, the data signal carrying audio data a sample of which is transferred via the system bus across at least two frames.

Regarding claim 9, which recites wherein said data signal includes control data for controlling a characteristic of the at least one peripheral device, traverse this rejection for at least the reasons provided above in connection with claim 7. The two-wire I^2C bus described in Kerns does not correspond to the claimed system bus. Further, Kerns concedes that "the I^2C protocol is not optimized for either high data rates or low power requirements and is therefore not well-suited for exchanging digital audio data." Col. 3, ll. 23-35.

Regarding claims 14-16, which as amended call for, *inter alia*, the portable communication device of claim 1 *further including* a wireless interface, Applicants traverse these rejections. The Office Action identifies elements 219 and 243 as apparently corresponding to a wireless interface. First, the switch 243 is clearly external to the hearing device 210, and claim

14 calls for the portable communication device to *include* a wireless interface. Second, the Office Action cites column 2, lines 63-65, which states that "the **auxiliary** device 240 operates to receive and optionally transmit real-time data, in particular digital audio signals" and column 3, lines 46-56, which describes the structure "Within the **auxiliary** device 240." Regarding claim 16, the Office Action cites column 2, lines 57-59, which states that the "**auxiliary** device 240 realizes a wired or wireless communication link for delivering audio information to the hearing device 210." However, the "auxiliary" device 240 is clearly external to the hearing device 210 (see FIG. 2). Regarding the interface chip 219, FIG. 3 is a "more detailed block diagram of the interface circuit of FIG. 2," and there is clearly no wireless interface shown there nor described anywhere in Kerns.

Regarding claim 20 as amended, which recites the portable communication device of claim 1, further including an external interface, said external interface being coupled to an external system bus that includes at least two signal-carrying lines, one of said lines carrying a digital signal and at least one other electrical signal between at least one external master component and an external peripheral device that includes an electro-mechanical or electro-acoustical component, said external system bus being communicatively coupled to said system bus via said external interface, Applicants traverse this rejection. The Office Action identifies the CLOCK line and the DATA line as corresponding to an external composite line adapted to carry more than one digital signal between at least one external master component (element 241) and an external peripheral device. However, as set forth above, the CLOCK and DATA lines each carry clock and data signals only and do not carry a digital signal and at least one other electrical signal. Kerns nowhere discloses that the CLOCK and DATA lines carry anything other than a clock signal and a data signal, respectively.

Regarding claim 23 as amended, which recites wherein said digital signal is a data signal that includes control data for controlling a characteristic of said at least one peripheral device, Applicants traverse the rejection. The DATA line in Kerns carries a data signal only and nothing else. It does not carry control data and at least one other electrical signal.

Regarding claim 24 as amended, which recites wherein said digital signal is a data signal that includes digital audio data, Applicants traverse the rejection. The DATA line in Kerns carries a data signal only and nothing else. It does not carry digital audio data and at least one other electrical signal.

Section 103 Rejections

Claims 5, and 10-12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kerns. Because claims 5 and 10-12 depend from claim 1, they are allowable for at least the same reasons that claim 1 is allowable. Applicants traverse the rejections for at least the following additional reasons.

Claim 10 recites the portable communication device of claim 7, wherein said at least one data slot is programmable by said master component to include a plurality of data slots. The Office Action concedes that Kerns does not disclose such a programmable data slot, but argues that it is obvious to one skilled in the art to modify or program one data slot that includes a plurality of data slots. Applicants respectfully disagree. FIGS. 4a-4c of Applicants' specification represent three different modes (dual, triple, and free slot modes) that each offer a flexible way to trade-off between the number of available slots and the precision of the data that is being communicated. Adding this kind of flexibility within the same synchronization scheme would not have been obvious to one of ordinary skill in the art but for Applicants' invention.

Claims 5 and 11-12 specify a range of values for a resistor coupled to said system bus (claim 5), and a range of values for power consumption of the system bus (claim 11) and the portable communication device (claim 12). The Office Action concedes that Kerns fails to disclose the resistor value ranges, the power consumption of the system bus, and the total power consumption of the portable communication device, but argues that it would be obvious to one skilled in the art that these components must be coupled to the system bus in order to operate and that furthermore, the selected range of resistor and power consumption values relies solely on design choices. Applicants respectfully traverse these rejections and lines of reasoning.

The resistor values represent a compromise between system speed and power consumption; they were not selected as a matter of design choice. In one embodiment, the resistor forms a passive pull down to hold the system bus at 0 volts, but its value is too high to actually ground the system bus fast enough. An active pull-down scheme is also contemplated for increased system speed, in which the "Bus Error" signal (¶ 57 of Applicants' disclosure) "always ends in logical zero." The combination of a high resistor pull-down for low-power consumption and an active pull-down scheme for increased system speed would not have been obvious to one of ordinary skill in the art.

Claims 17 and 18 (which depends from claim 17) were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kerns in view of U.S. Patent Application Publication No. 2003/0206237 A1 (Imaizumi). The Office Action asserts that Imaizumi discloses in the Abstract an image processing apparatus in which each data bit transmitted is sampled twice, but Applicants respectfully disagree and traverse these rejections. First, Imaizumi is non-analogous art as it pertains to image processing apparatuses and not portable communication devices. One of ordinary skill in the art of portable communication devices would not be motivated to draw

upon the teachings in the art of image processing. In any event, the "correlated double sampling circuit" converts **analog** photoelectric signals to the digital domain. In fact, the output of the CDS circuit is "gain-controlled by an automatic gain control (AGC) circuit *then A/D converted by an A/D converter into a digital signal*, and inputted into a digital signal processing circuit (DSP)." Imaizumi, ¶ 54. Thus, the CDS circuit in Imaizumi is not capable of double-sampling a data **bit**, which by definition is digital, because its input is an analog signal and its output is an analog signal, not data bits. The conventional CDS circuit disclosed in Imaizumi operates upon an **analog** video signal. Accordingly, Applicants submit that a prima facie case of obviousness has not been made, and respectfully request allowance of claims 17-18.

Conclusion

Applicants respectfully submit that the claims are in condition for allowance and such action is earnestly solicited. If there are any matters which may be resolved or clarified through a telephone interview, the Examiner is respectfully requested to contact Applicants' undersigned attorney at the number indicated.

Checks in the amounts of $450.00 and $100.00 to cover fees for a Petition for Two-Month Extension of Time and the additional claims are submitted herewith. It is believed that no additional fees are presently due; however, should any additional fees be required (except for payment of the issue fee), the Commissioner is authorized to deduct the fees from Deposit Account No. 10-0447 (47161-00041USPT) for any fees inadvertently omitted which may be necessary now or during the pendency of this application, except for the issue fee.

Respectfully submitted,

Date: April 14, 2006

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